# EE 434
# Lecture 2

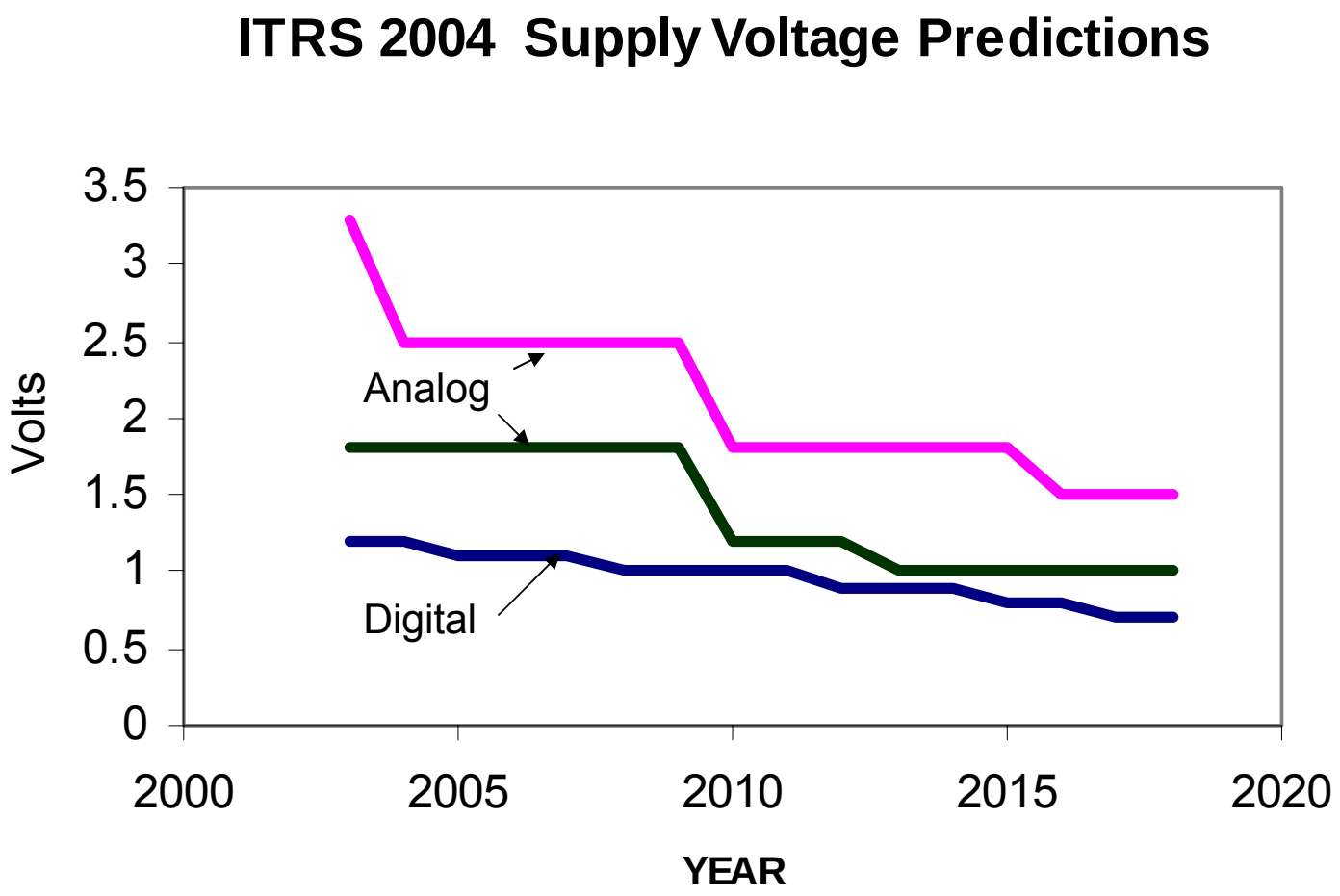
## Basic Concepts

## Review from Last Time

- Semiconductor Industry is One of the Largest Sectors in the World Economy and Growing
- All Initiatives Driven by Economic Opportunities and Limitations
- Rapidly Growing Device Count and Rapidly Shrinking Feature Sizes (Moore's Law?)
- Designers Must Handle Incredible Complexity Yet Work in Large Teams and Make Almost No Mistakes
- Understand the Big Picture and Solve the Right Problem

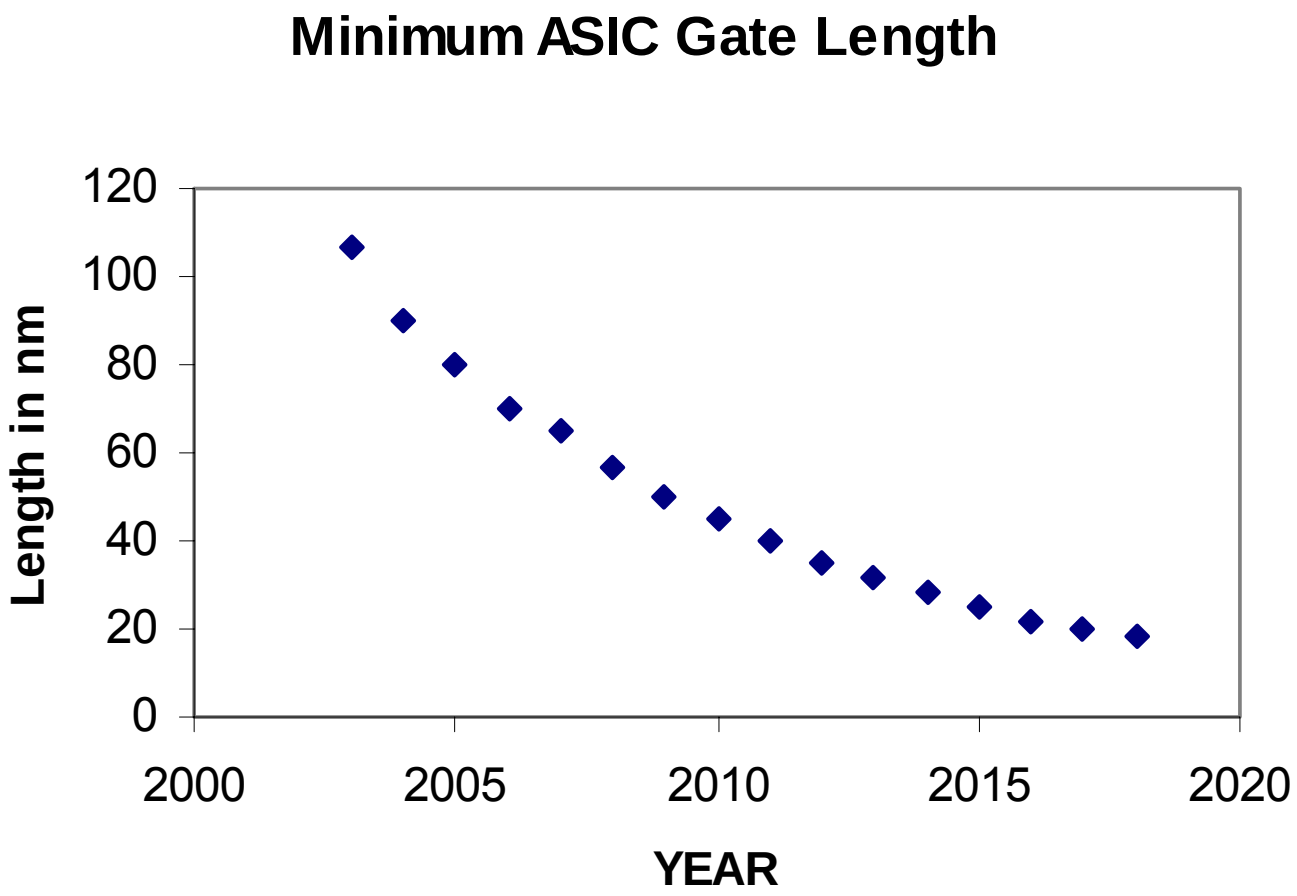
Review from Last Time

# ITRS Technology Predictions



Review from Last Time

# ITRS Technology Predictions



# How can complex circuits with a very large number of transistors be efficiently designed with low probability of error?

- Many designers often work on a single design
- Single error in reasoning, in circuit design, or in implementing circuit on silicon generally results in failure
- Design costs and fabrication costs for test circuits are very high
  - Design costs for even rather routine circuits often a few million dollars and some much more
  - Masks and processing for state of the art processes often between $1M and $2M
- Although much re-use is common on many designs, considerable new circuits that have never been designed or tested are often required
- Time to market critical – missing a deadline by even a week or 2 may kill the market potential

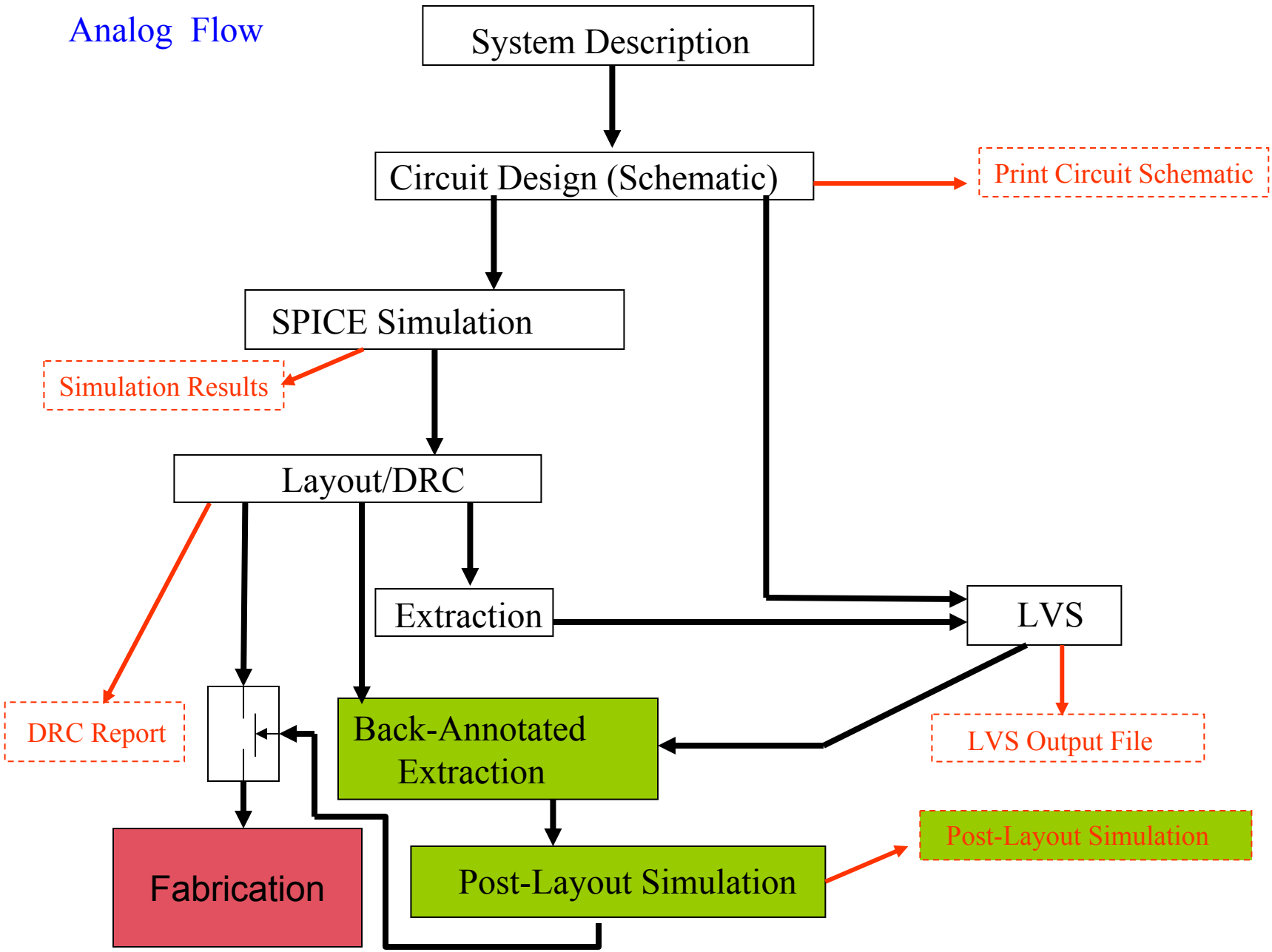
# How can complex circuits with a very large number of transistors be efficiently designed with low probability of error?

- CAD tools and CAD-tool environment critical for success today
- Small number of VLSI CAD toolset vendors
- CAD toolset helps the engineer and it is highly unlikely the CAD tools will replace the design engineer
- Major emphasis in this course on using toolset to support the design process

# CAD Environment for Integrated Circuit Design

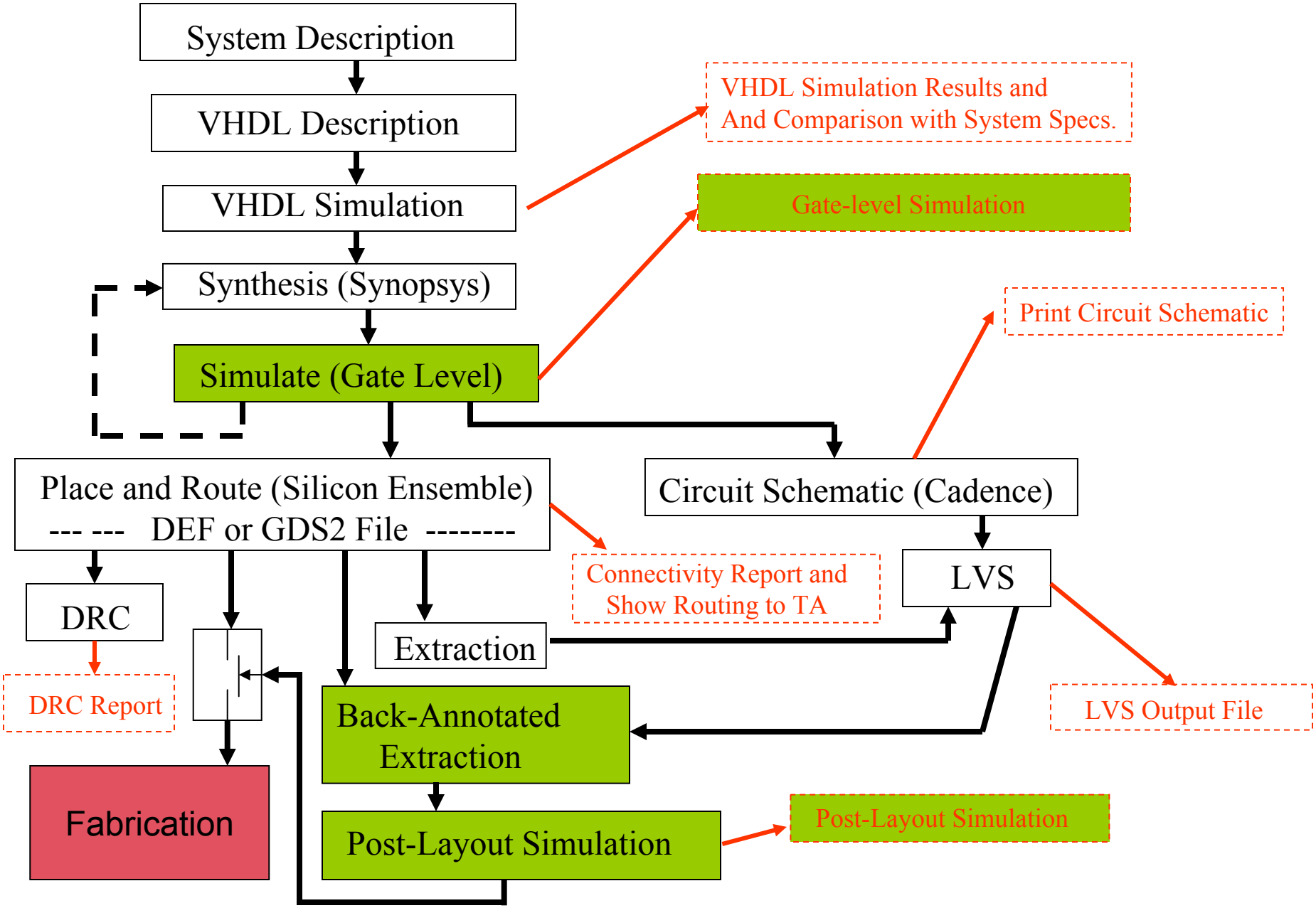
- Typical Tool Flow
  - (See Chapter 8 of Text)
- Laboratory Experiments in Course

# VLSI Design Flow Summary



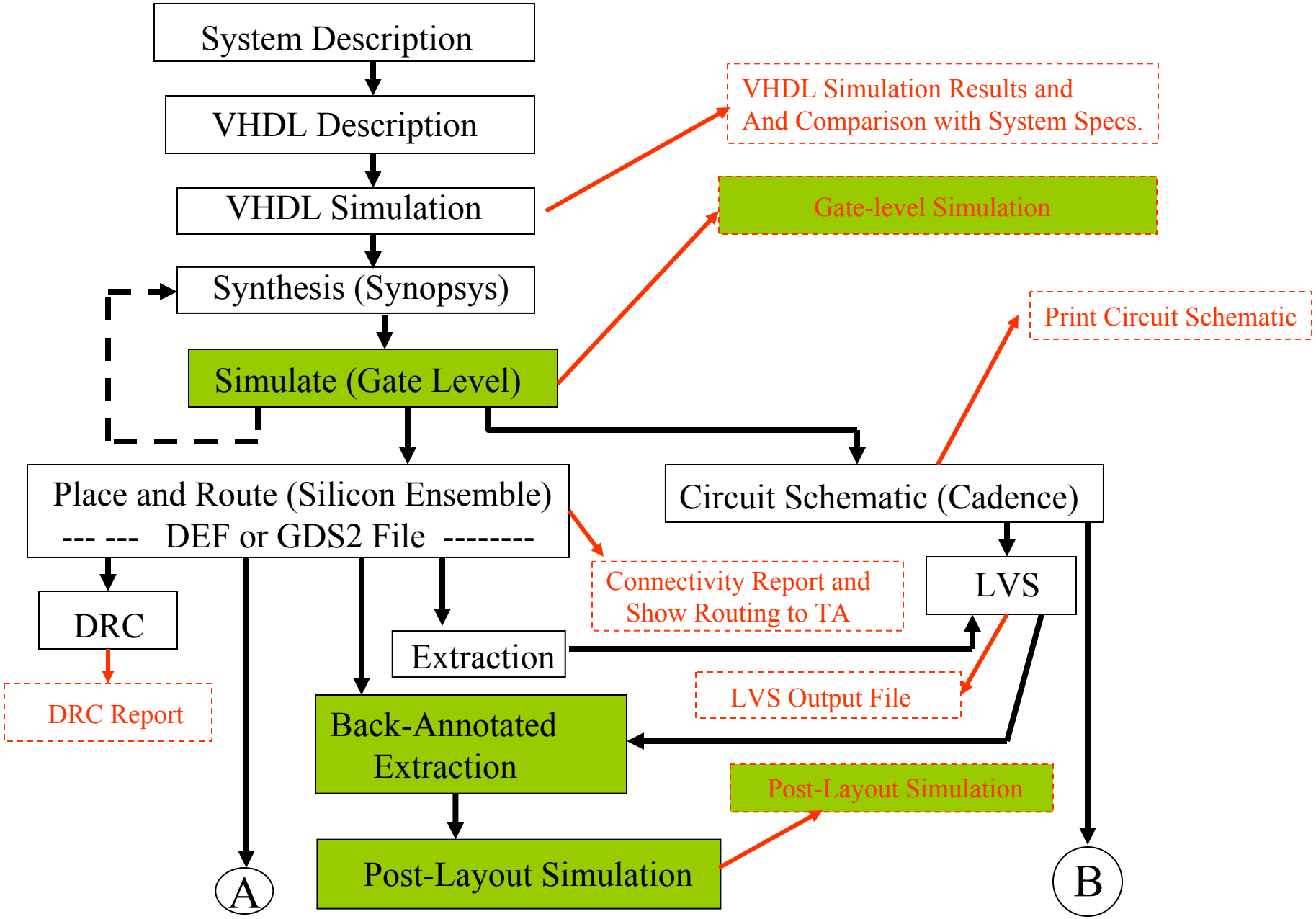
# VLSI Design Flow Summary

Digital Flow



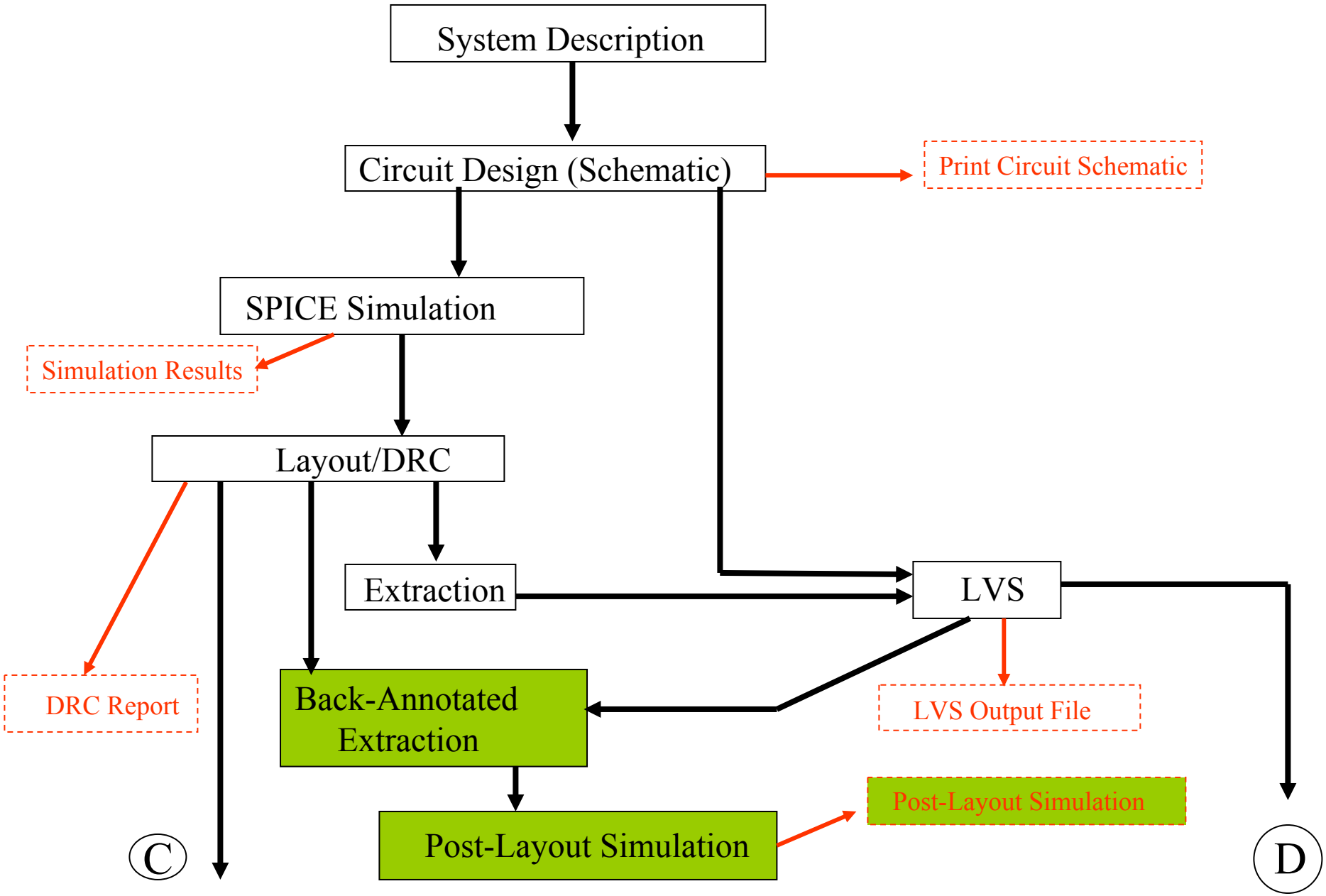
# VLSI Design Flow Summary

Mixed Signal Flow (Digital Part)



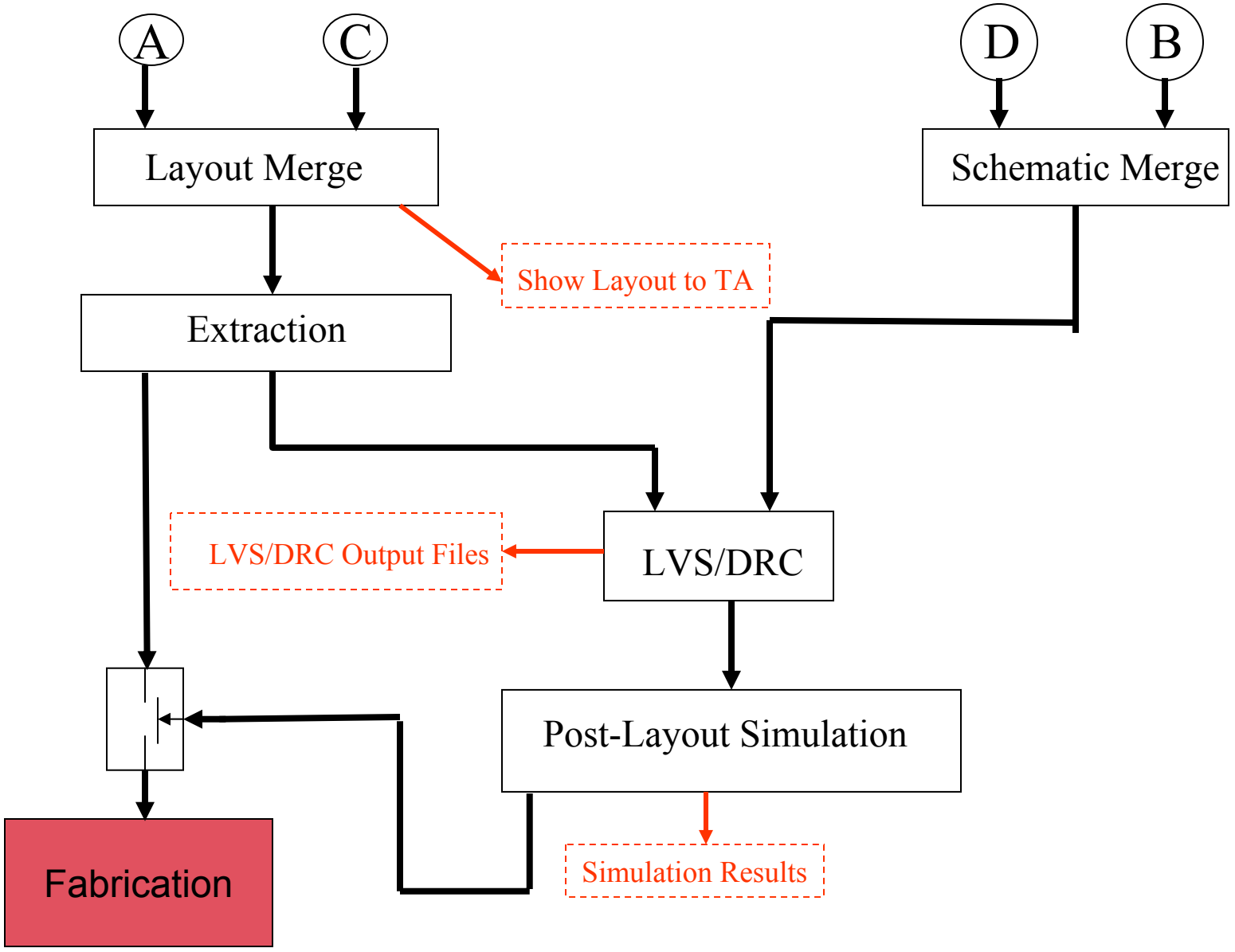
# VLSI Design Flow Summary

## Mixed-Signal Flow (Analog Part)



# VLSI Design Flow Summary

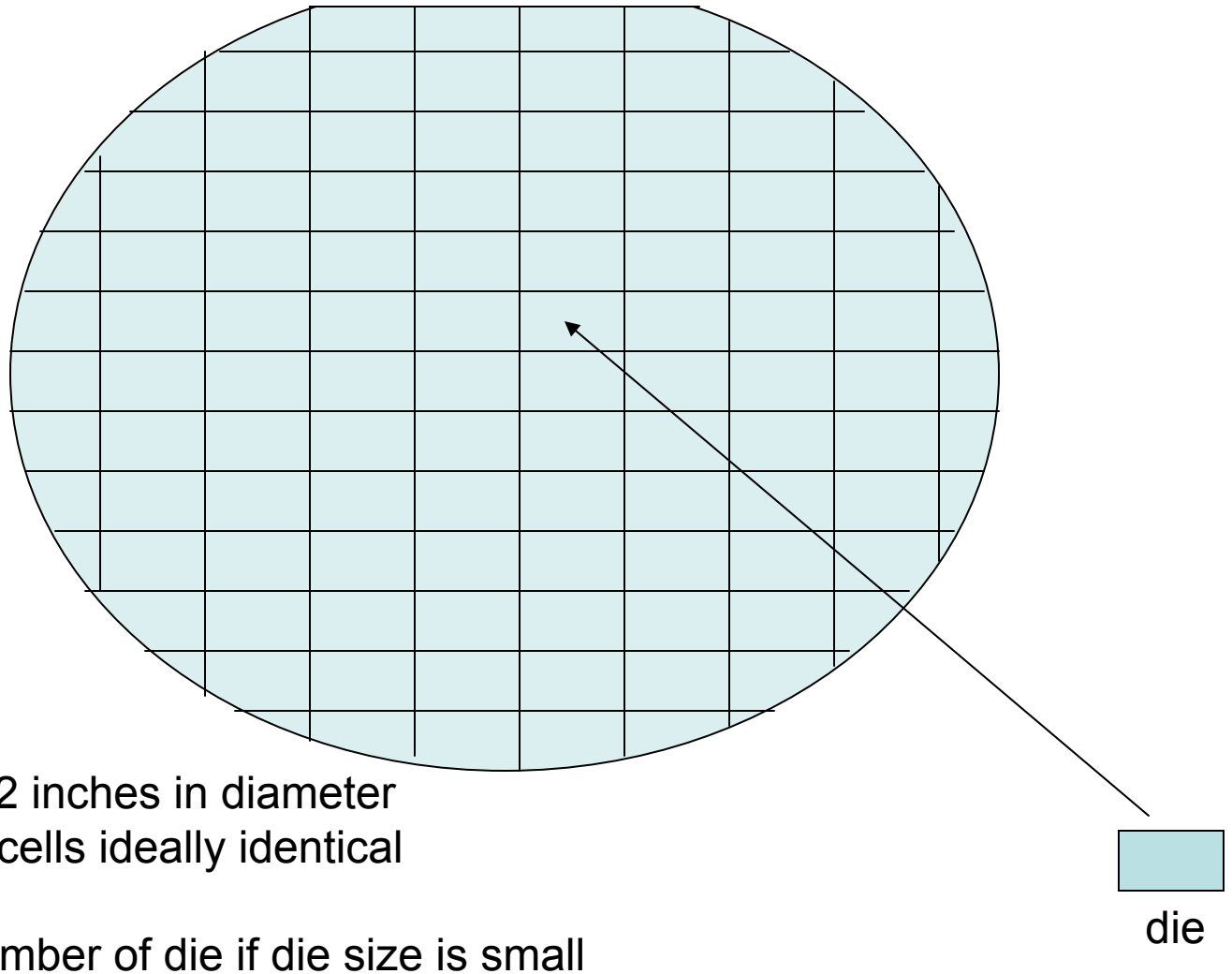
## Mixed-Signal Flow (Analog-Digital Merger)



# Comments

- The Analog Design Flow is often used for small digital blocks or when particular structure or logic styles are used in digital systems
- Variants of these flows are widely used and often personalized by a given company or for specific classes of circuits

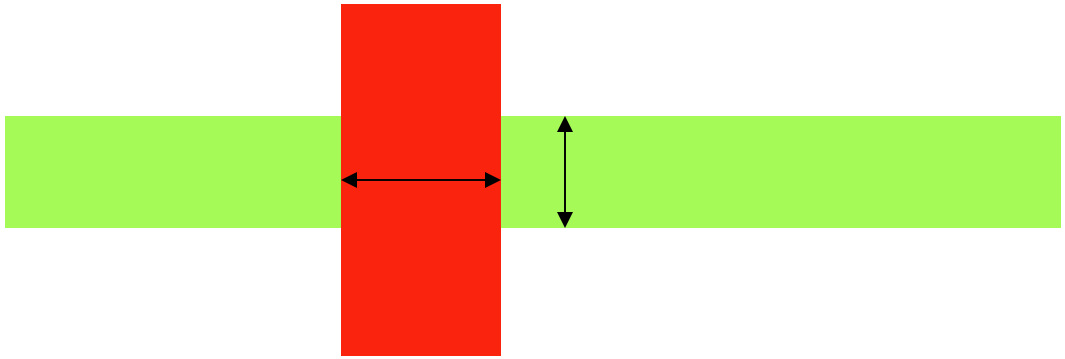
# Wafer




- 6 inches to 12 inches in diameter
- All complete cells ideally identical
- flat edge
- very large number of die if die size is small

# Feature Size

Feature size is the minimum lateral feature size that can be **reliably** manufactured



Often given as either feature size or pitch

Minimum feature size often identical for different features

# What is meant by “reliably”

Yield is acceptable if a very large number of these features are made

If P is the probability that a feature is good

n is the number of features on an IC

Y is the yield

$$Y = P^n$$

$$P = e^{\frac{\log_e Y}{n}}$$

# Example: How reliable must a feature be?

n=5E3

Y=0.9

$$P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E3}}$$ **=0.999979**

But is n=5000 large enough ?

More realistically n=5E9

$$P = e^{\frac{\log_e Y}{n}} = e^{\frac{\log_e 0.9}{5E3}}$$ **=0.999999999979**

**Extremely high reliability must be achieved in all processing steps to obtain acceptable yields in state of the art processes**

# Feature Size

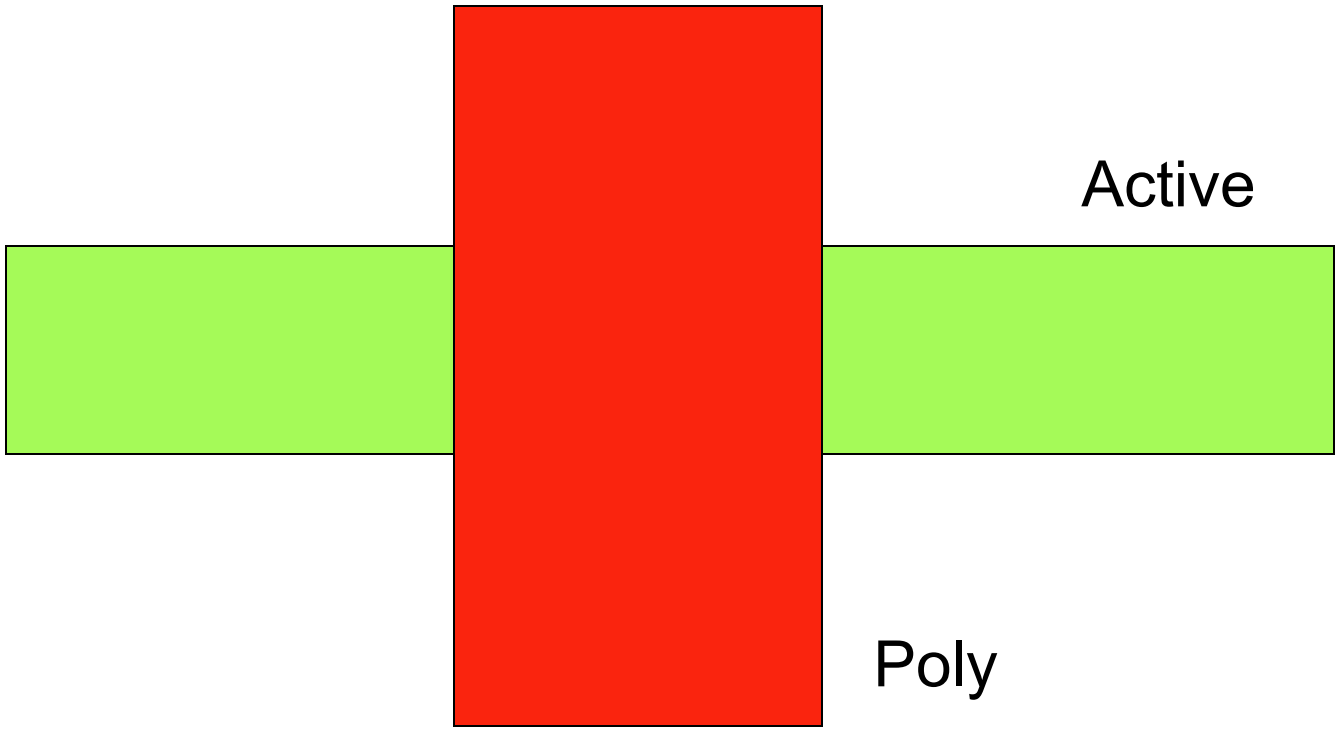
- Typically minimum length of a transistor
- Often minimum width or spacing of a metal interconnect (wire)
- Point of “bragging” by foundries
  - Drawn length and actual length differ
- Often specified in terms of pitch
  - Pitch approximately equal to twice minimum feature size

# Feature Size Evolution

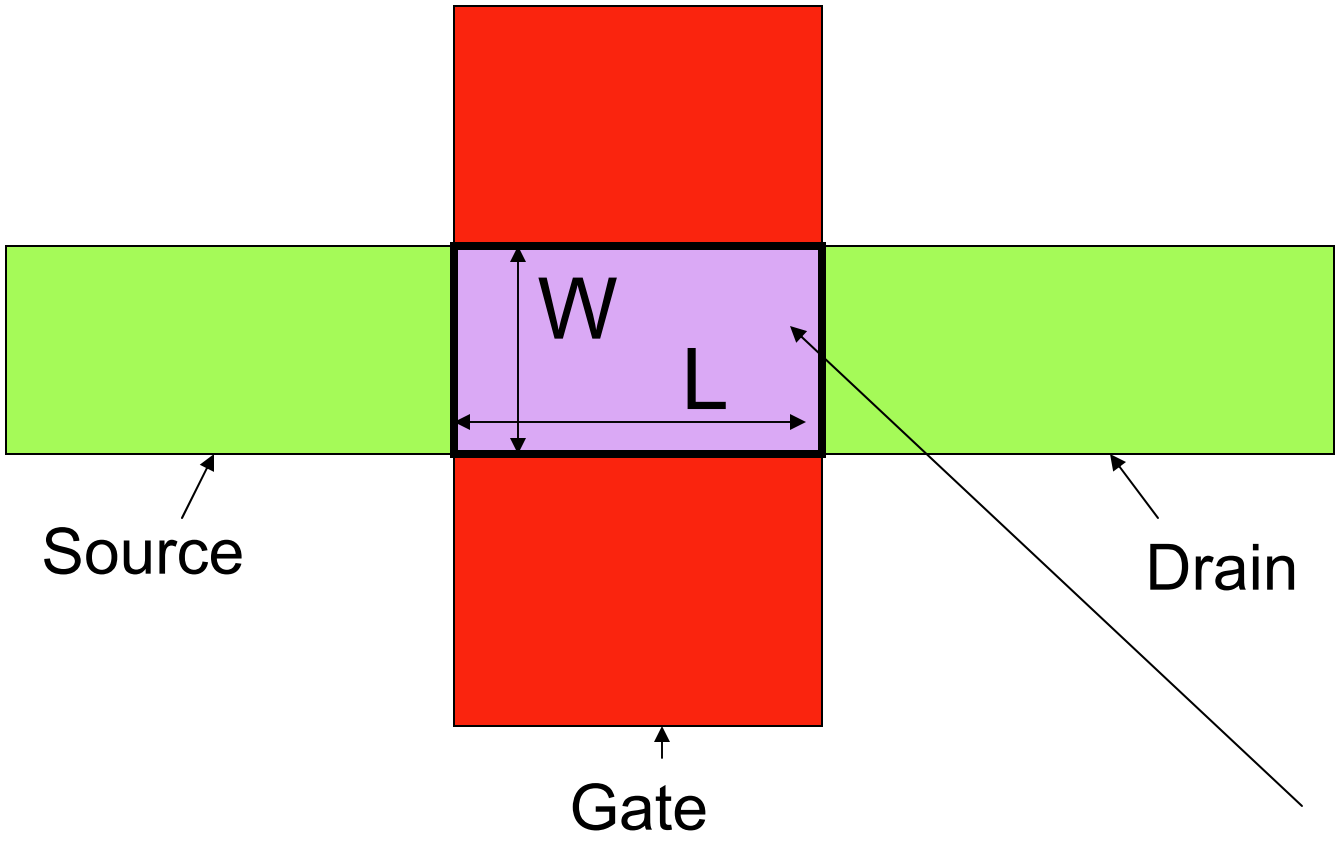
| | |
|---|---|
| Mid 70's | 25μ |
| 2005 | 90nm |
| 2010 | 45nm |
| 2020 | 20nm |

$$1\mu = 10^3\, nm = 10^{-6}\, m = 10^4\ \mathring{\mathrm{A}}$$

# MOS Transistor

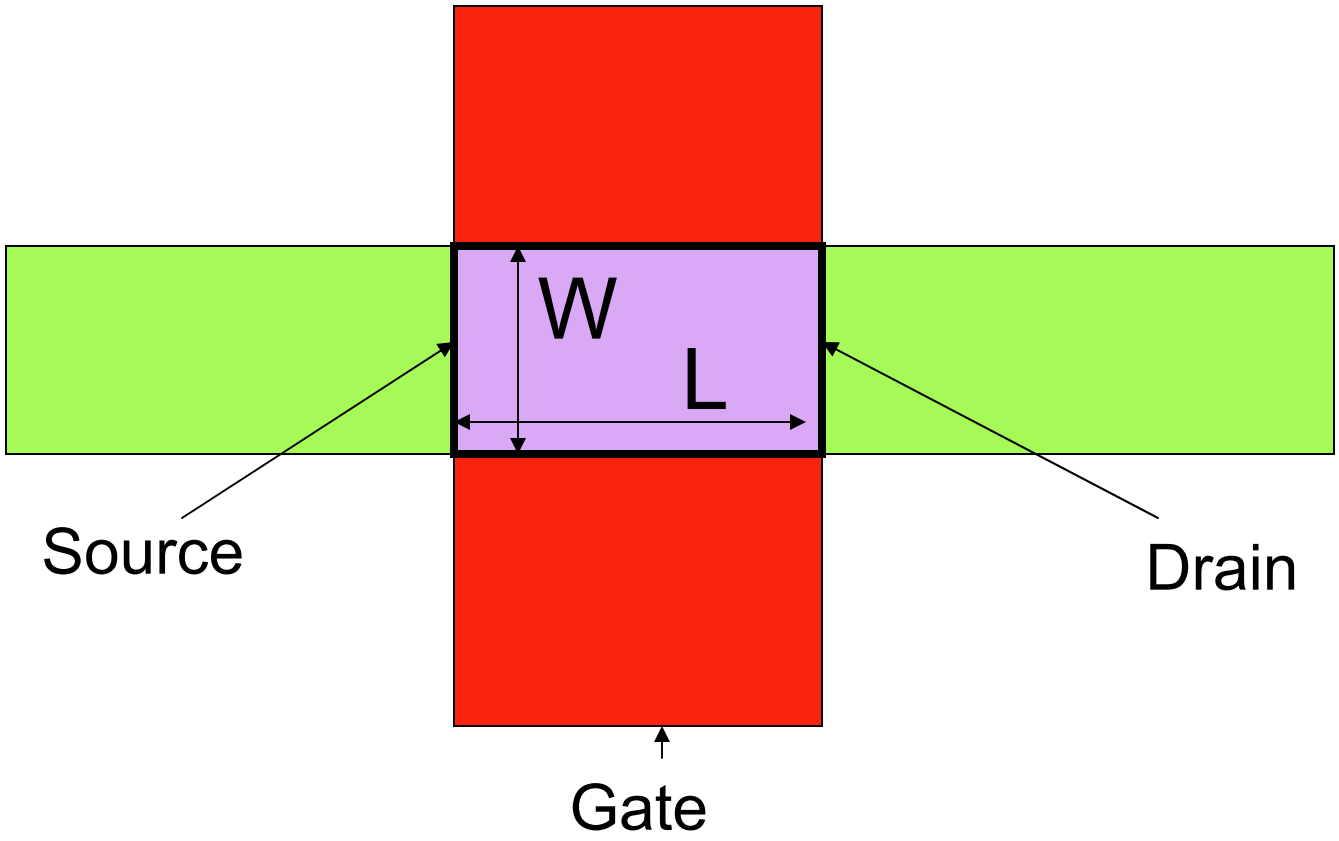


# MOS Transistor



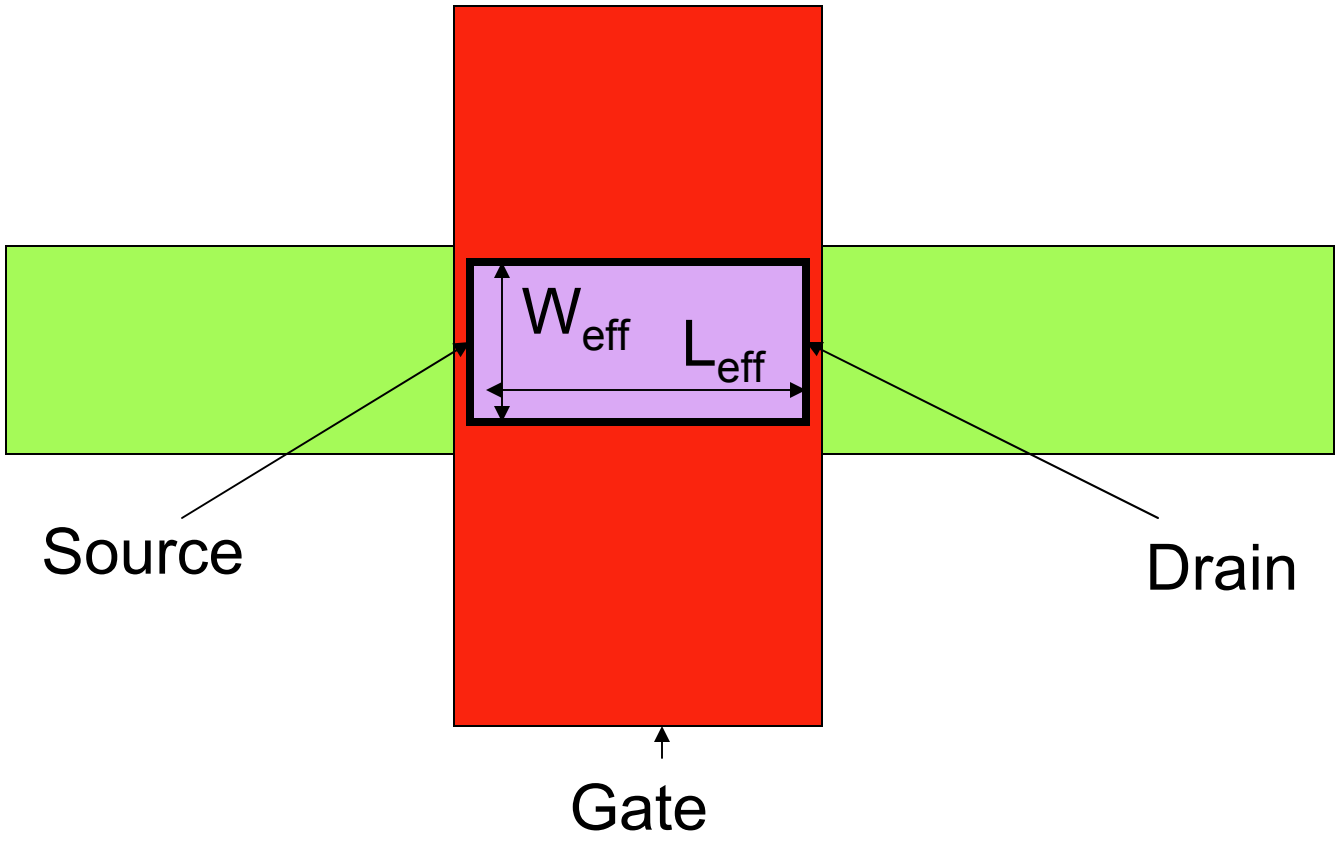

Drawn Length and Width Shown

# MOS Transistor




Actual Drain and Source at Edges of Channel

# MOS Transistor




Effective Width and Length Generally
Smaller than Drawn Width and Length

# Technology Nomenclature

- SSI Small Scale Integration 1-100
- MSI Medium Scale Integration $100\text{-}10^3$
- LSI Large Scale Integration $10^3\text{-}10^5$
- VLSI Very Large Scale Integration $10^5\text{-}10^6$

Any design in a process capable of incorporating a large number of devices is generally termed a VLSI design

# Device and Die Costs

Consider the high-volume incremental costs of manufacturing integrated circuits

Example: Assume an 8” wafer in a 0.25μ process costs $800

Determine the number of minimum-sized transistors that can be fabricated on this wafer and the cost per transistor. Neglect spacing and interconnect.

Solution:

$$n_{trans} \cong \frac{A_{wafer}}{A_{trans}} = \frac{\pi(4in)^2}{(0.25\mu)^2} = 5.2E11$$

$$C_{trans} = \frac{C_{wafer}}{n_{trans}} = \frac{\$800}{5.2E11} = \$15.4E-9$$

Note: the device count may be decreased by a factor of 10 or more if Interconnect and spacing is included but even with this decrease, the cost per transistor is still very low!

# Device and Die Costs

$$C_{per\ unit\ area} \cong \$2.5 / cm^2$$

Example: If the die area of the 741 op amp is 1.8mm$^2$, determine the cost of the silicon needed to fabricate this op amp

$$C_{741} = \$2.5 / cm^2 \bullet \left(1.8mm^2\right) \cong \$.05$$

Actual integrated op amp will be dramatically less if bonding pads are not needed

End of Lecture 2